UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/631,856	08/01/2003	Yasushi Kasa	100353-00172	9168

4372 7590 07/05/2005

ARENT FOX PLLC
1050 CONNECTICUT AVENUE, N.W.
SUITE 400
WASHINGTON, DC 20036

EXAMINER	
NGUYEN, TAN	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 07/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/631,856	KASA ET AL.
	Examiner	Art Unit
	Tan T. Nguyen	2827

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4 and 7* is/are rejected.

7)☒ Claim(s) *2-3, 5-6* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. The R.C.E. submitted by Applicants on May 11, 2005 has been received.

2. The Information Disclosure Statement submitted by Applicants on May 11, 2005 has been received and fully considered.

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1, 4 and 7 are rejected under 35 U.S.C. 102(b) as being anticipated by Keeney (U.S. Patent No. 5,798,966).

Kenney disclosed in Figure 4 a nonvolatile memory device having a memory array [400] having four separately addressable memory blocks [402-405] (column 9, lines 26-27). A drain voltage generator [308] may adjust the bit line voltage applied to bit line [406] to compensate for the bit line resistance that exists between the drain voltage generator [308] and the selected memory block that includes a selected memory cell. Similarly, source voltage generator [312] may also adjust the source line voltage applied to source line [424] to compensate for the source line resistance that exists between the source line voltage generator [312] and the selected memory block that includes a selected memory cell (column 9, lines 32-40). In Figures 5-6, Kenney further disclosed once drain voltage generator [308] and source voltage generator [312] have determined the appropriate bit line and source line voltages to apply to the bit line and the source line, respectively, of a selected memory cell, then the selected memory cell may be programmed using various known programming method (column 9, lines

41-45). By adjusting the bit line and source voltages to compensate for voltage drops due to the bit line and source line resistance, the actual drain to source (VDS) voltage across the terminal of each selected memory cell in the memory array may be controlled to be substantially constant or uniform throughout the memory array (column 9, lines 53-60). In Figures 6-7, Keeny disclosed the drain voltage generator [600] and the source voltage generator [700], each have a block offset memory [602], [702] and a location offset memory [604], [704] coupled to voltage generator [608], [708] (column 11, lines 51-53, column 12, lines 23-25). The block offset memory [602] , [702] decode the block address for the selected memory cell (column 11, lines 58 to column 12, line 2), the location offset memory [604], [704] decode the address for the selected memory cell within the selected block of memory (column 12, lines 3-7). The voltage generator [608], [708] receive the values from block offset memory [602], [702] and location offset [604], [704] and generate bit line voltage [HHVPW] (column 12, lines 18-20) and source line voltage [VPS] (column 12, lines 43-47). Either of the drain voltage generator [600] or the source voltage generator would be considered as the claimed program potential generating circuit since both the drain voltage generator [600] and the source voltage generator [700] adjust the voltage for programming in according to the position of the memory cell in the selected block.

Regarding claim 4, the combination of either of the block offset memory [602]/[702] and the memory offset memory [604/704] would be understood as the claimed program potential adjusting circuit since these circuit storing the value indicating the offset voltages at addresses that are accessed, or having program that

calculates the offset voltages in response to the address received on the address buses (column 12, lines 11-16).

Regarding claim 7, as shown in Figure 4, the memory array [400] includes four memory blocks [402-405] arranged at different distances in respect to the drain and source voltage generator [302] and [[308]. The block offset memory [602], [702] decode the block address of the selected block, and the location offset memory decodes the address of the selected memory within the selected block to control the voltage generator [608], [708] to generate appropriate voltage in respect with the location of the selected memory cell.

5. Claims 2-3, 5-6 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The prior art failed to show or suggest the booster circuit and the regulator circuit as claimed in claims 2-3, the program potential adjusting circuit which generates a program potential adjusting signal, or how the program potential adjusting circuit perform inversion control as claimed in claims 5-6).

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. ***

Kobayashi et al. is cited to show a nonvolatile memory device having a plurality of blocks.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tan T. Nguyen whose telephone number is (571) 272-

1789. The examiner can normally be reached on Monday to Friday from 07:00 AM to 03:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hoai Ho, can be reached at (571) 272-1777. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tan T. Nguyen
Primary Examiner
Art Unit 2827
June 30, 2005